REMARKS

By this submission accompanying with a request for continued examination, claims 5-8 are amended. No new matter is contained in the amendments. Accordingly, claims 1-8 are pending in this application and claims 5-8 are respectfully submitted for a timely examination.

Allowed Claims

As a preliminary matter, Applicants appreciate the allowance of claims 1-4.

Drawing Objection

The drawings were objected to under 37 C.F.R. §1.83(a) because the Examiner took the position that the drawings failed to show every feature of the invention specified in the claims. In particular, the Examiner asserted that the drawings, as originally filed, failed to show the feature of "counting a number of the PLL clock signal" as recited in claim 5 of the present application.

Applicants respectfully traverse the objection and submit that the drawings of the present application do indeed show every feature recited in claim 5. In particular, Applicants highlight Figures 5 and 7 of the present application.

Figs. 5 and 7 illustrates one embodiment of the present invention where, for example, the second flip-flop group 45 counts a number of the PPL clock signal as recited in claim 5. When a cable is connected in the present invention, the select signal Select becomes L level which causes the counter 44 to start counting and then signal CLKSEL becomes L level after the counting by the counter 44. The counter 44 counts the basic clock X'tal. One reason the counter 44 counts is to allow the circuit to wait until the PLL becomes stable after the select signal Select becomes L level that causes

the PLL to start generating the clock. Then, the signal CLKSEL=L is provided to the first flip-flop group 43 and the inverted signal of CLKSEL is then provided to the second flip-flop group 45. The first flip-flop group 43 causes the basic clock to disappear within one basic clock (see t35 in Fig. 7). On the other hand, the second flip-flop group 45 for instance transfers the inverted CLKSEL through plural flip-flops in sync with the fast PLL clock. After transferring the inverted CLKSEL(=H), the second flip-flop group 45 allows outputting the fast PLL clock through AND2. The transfer of the inverted CLKSEL(=H) corresponds to the counting of a number of the PLL clock through a predetermined number of flip-flops.

Accordingly, Applicants submit that Figure 5 and in particular Figure 7 of the present application indeed support every feature recited in claim 5, and therefore respectfully request withdrawal of the objection.

Claim 5 Rejected Under 35 U.S.C. § 112, 1st Paragraph

Claim 5 was rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement. In making this rejection, the Examiner took the position that "neither the specification nor the drawing as originally presented supports" the limitation of "counting a number of the PLL clock signal" as recited in claim 5 of the present application.

Applicants submit that the remarks as set forth in the above section are responsive to this rejection. In particular, it is submitted that the pages of the present specification corresponding to the description of Figures 5 and 7 indeed support the limitations recited in claim 5. Thus, Applicants request withdrawal of the rejection.

Claim 6 Rejected Under 35 U.S.C. § 112, 1st Paragraph

Application No.: 09/713,024
Attorney Docket No.: 108066-00018

The Office Action rejected claim 6 under 35 U.S.C. § 112, first paragraph as being non-enabling. Claim 6 has been amended to obviate this rejection.

Claims 7-8 Rejected Under 35 U.S.C. § 102(b)

The Office Action rejected claims 7-8 under 35 U.S.C. § 102(b) as being anticipated by Parmenter et al. (U.S. Patent No. 5,679,353, hereinafter "Parmenter"). Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 7 recites a clock signal switching circuit comprising, among other features, an inhibiting circuit including a first circuit for disappearing the basic clock as the output when the switching said output from said basic clock to said fast clock, and a second circuit for inhibiting the fast clock until the basic clock disappears through the first circuit and for allowing the output of the fast clock when the switching said output from said basic clock to said fast clock.

Claim 8 recites a clock signal switching circuit comprising, among other features, an inhibiting circuit including a first circuit for disappearing the basic clock as the output when the switching said output from said basic clock to said fast clock, and a second circuit for inhibiting the fast clock until the basic clock disappears through the first circuit and for allowing the output of the fast clock when the switching said output from said basic clock to said fast clock.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

In making the rejection, the Examiner characterized the "multiplexers and their associated control means (figure 2, structures 19, 21, and their control means structure SR1)" of Parmenter as allegedly being comparable to the feature of "inhibiting circuit that inhibits said fast clock ..." recited in claims 7 and 8 of the present application.

Applicants respectfully disagree and traverse the Examiner's position.

Parmenter merely discloses that the multiplexers 19 and 21 switch between the basic clock CLK2 and the fast PLL clocks 1X_CLK2 and 2X_CLK2 when the PLL is unlocked condition and locked condition. In particular, Fig. 1 of Parmenter shows the locked condition signal PLL LOCK for controlling the multiplexer MUX. Further, Parmenter provides that such switching is executed without generating glitches and loss-of-state during the mode transition. Therefore, the control of Parmenter waits until the next clock phase boundary to change the clock mode. (See col. 2, lines 44-47 and the last line of claim 1.) Therefore, Applicants submit that Parmenter fails to disclose or suggest at least the inhibiting circuit having the first and second circuit as recited in claims 7 and 8, and further submit that claims 7 and 8 are allowable.

Claim 5 Rejected Under 35 U.S.C. § 102(b)

The Office Action rejected claim 5 under 35 U.S.C. § 102(b) as being unpatentable over Yokogawa et al. (U.S. Patent No. 4,872,155, hereinafter "Yokogawa") in view of Ishikawa (U.S. Patent No. 6,346,830). Applicants respectfully traverse the rejection on the grounds that the rejection is improper, and on the grounds that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

As a preliminary matter, Applicants submit that the rejection is improper as citing

multiple references under a 35 U.S.C. § 102 rejection. Specifically, the rejection of

claim 5 is based on 35 U.S.C. § 102(b) as being unpatentable over two references,

them being Yokogawa in view of Ishikawa.

According to MPEP, section 2131.01 states,

> Normally, only one reference should be used in making a
> rejection under 35 U.S.C. 102. However, a 35 U.S.C. 102
> rejection over multiple references has been held to be proper
> when the extra references are cited to:
>
> (A) Prove the primary reference contains an "enabled
> disclosure;"
> (B) Explain the meaning of a term used in the primary
> reference; or
> (C) Show that a characteristic not disclosed in the reference
> is inherent.

It is submitted that the rejection over multiple references is not proper since the

extra reference of Ishikawa was cited to supplement a deficiency in Yokgawa. In

particular, the Office Action noted that,

> [A]although Yokogawa discloses the PLL circuit for
> comparing phases of different clock's speeds (column 4,
> lines 47-49), Yokogawa does not explicitly disclose that the
> PLL clock is faster than the clock speed as the amended
> claim recites.
>
> Ishikawa discloses an I/O interface with PLL circuits for
> supporting different I/O clock speeds (figure 5). Ishikawa
> teaches one to synchronize the clock speed in response to
> data output and data input with different PLL speeds (column
> 2, lines 53-67, column 3, lines 1-30). ...
>
> Hence, it would have obvious to one having ordinary skill in
> the computer art at the time Applicant made the invention to
> adapt the Ishikawa's teaching onto Yokogawa because
> Ishikawa teaches one to establish a reliable data reception
> by establishing the value of data at a particular phase of the

clock with two separate PLLs synchronizing both input data speed and output data speed.

It is submitted the extra reference of Ishikawa neither (A) Prove the primary reference contains an "enabled disclosure;" (B) Explain the meaning of a term used in the primary reference; nor (C) Show that a characteristic not disclosed in the reference is inherent. Therefore, Applicants submit that the rejection is improper and respectfully request that the rejection be withdrawn, and the allowance of claim 5.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 5-8 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 5-8 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time.

Application No.: 09/713,024
Attorney Docket No.: 108066-00018

Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referring to client-matter number 108066-00018.

Respectfully submitted,

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Enclosure: Petition for Extension of Time (two months)

Application No.: 09/713,024
Attorney Docket No.: 108066-00018